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| EWULogo.png | | **EAST WEST UNIVERSITY** | | |
| **Department of Computer Science and Engineering** | | |
| **B.Sc. in Computer Science and Engineering Program** | | |
| **Mid Term II Examination, Summer 2019 Semester** | | |
| **Course:** | | **CSE442 Microprocessors and Microcontrollers, Section-3** | |  |
| **Instructor:** | | **Anika Tabassum** | |  |
| **Full Marks:** | | **40** | |  |
| **Time:** | | **1 Hour and 20 Minutes** | |  |
| **Note:** There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Marks of each question are mentioned at the right margin. | | | | |
| 1. | **Design** a 64Kx8 ROM chip. Write the pins and their functions in tabulated form. | | [CO2, C3, Mark: 4] | |
| 2. | **Design** an interface between a memory 2716EPROM and Intel 8088 microprocessor using a NAND gate decoder. Calculate the memory location decoded by NAND gate. Determine the inputs of the control signals for reading data. | | [CO2, C3, Mark: 8] | |
| 3. | **Analyze** the diagram in figure 1 and determine the addresses of PORT A, PORT B and PORT C. | | [ CO2, C3, Mark: 6] | |
|  | Figure. 1 | |  | |
| 4. | Determine the command bytes for the following operations-   1. Set the value at PORT C to 2H 2. GROUP A operating on MODE 1 as I/P port, GROUP B operating on MODE 0 as O/P port | | [ CO2, C3, Mark: 8] | |
| 5. | **Analyze** the clock generator 8284A for 8086/8088 microprocessor given in Figure 2. What would be the output-   1. When F/C=0 2. When F/C=1   Show the timing diagram for all input and output signals for both a) and b) separately.    **120 MHz** | | [CO2, C3, Mark: 6] | |
| 6. | |  |  | | --- | --- | | **Write** an assembly code to set the value of trap flag equal to 1. When is this needed? | | |  |  | | | [CO2, C3, Mark: 8] | |